In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (currently amended) A method for fabricating a semiconductor device, comprising:

forming a dielectric layer overlaying a semiconductor substrate;

forming an opening in the dielectric layer;

embedding copper or copper alloy into the opening;

forming a silicon layer on the copper or copper alloy by sputtering; [[and]]

reacting the silicon layer with the underlying copper or copper alloy to form a copper silicide layer capping the surface of the copper or copper alloy;

removing un-reacted portions of the silicon layer; and

forming a diffusion barrier layer overlaying the copper silicide.

2. (original) The method as claimed in claim 1, wherein the dielectric layer comprises a low-k material having k value less than 3.2.

3. (original) The method as claimed in claim 1, wherein the dielectric layer comprises organic low-k material, CVD low-k material, a combination of organic low-k material and CVD low-k material, carbon-containing silicon oxide, nitrogen-containing silicon oxide, FSG, SiC, SiOC or SiOCN.

4. (original)The method as claimed in claim 1, wherein the width of the opening is less than 900Å.

5. (original)The method as claimed in claim 1, wherein the thickness of the embedded copper or copper alloy is less than 4000Å.

6. (original) The method as claimed in claim 1, wherein the silicon layer comprises amorphous silicon.

7. (original) The method as claimed in claim 2, wherein the thickness of the silicon layer is 50 to 500Å.

8. (original) The method as claimed in claim 1, wherein the copper or copper alloy is formed by the steps of:

depositing a copper seed layer in the opening; and

electro-chemical plating or electroless plating the copper or copper alloy on the copper seed layer.

9. (original) The method as claimed in claim 1, wherein the copper or copper alloy is formed by chemical vapor deposition.

10.(original) The method as claimed in claim 1, wherein the copper silicide layer is formed by subjecting the semiconductor substrate to an inert gas-containing ambience at a temperature of about 150 degrees C. to about 450 degrees C.

11. (cancelled)

12. (currently amended) The method as claimed in claim [[11]]1, wherein the diffusion barrier layer comprises silicon-rich oxide, SiN, SiC, SiOC, SiOCN, carbon-containing silicon oxide or nitrogen-containing silicon oxide.

13. (currently amended) The method as claimed in claim [[11]]1, further comprising a step of: forming an etch-stop layer overlaying the diffusion barrier layer.

14. (currently amended) The method as claimed in claim 13, wherein the etch-stop layer comprises silicon-rich oxide, SiC, SiOC, SiON, SiOCN, carbon-containing silicon oxide or nitrogen-containing silicon oxide.

15. (currently amended) The method as claimed in claim 13, ~~A method for fabricating a semiconductor device, comprising: forming a dielectric layer overlaying a semiconductor substrate; forming an opening in the dielectric layer; embedding copper or copper alloy into the opening;~~ wherein ~~forming a~~ the silicon layer is formed on the copper or copper alloy by chemical vapor deposition~~; and reacting the silicon layer with the underlying copper or copper alloy to form a copper silicide layer capping the surface of the copper or copper alloy~~.

16. (currently amended)The method as claimed in claim [[15]] 30, wherein the dielectric layer comprises a low-k material having k value less than 3.2.

17. (currently amended)The method as claimed in claim [[15]] 30, wherein the dielectric layer comprises an organic low-k material, a CVD low-k material, a combination of organic low-k material and CVD low-k material, carbon-containing silicon oxide, nitrogen-containing containing silicon oxide, FSG, SiC, SiOC or SiOCN.

18. (currently amended)The method as claimed in claim [[15]] 30, wherein the width of the opening is less than 900 .ANG..

19. (currently amended)The method as claimed in claim [[15]] 30, wherein the thickness of the embedded copper or copper alloy is less than 4000 .ANG..

20. (original) The method as claimed in claim 15, wherein the chemical vapor deposition is plasma-enhanced chemical vapor deposition.

21. (currently amended)The method as claimed in claim [[15]] 30, wherein the silicon layer comprises amorphous silicon.

22. (currently amended)The method as claimed in claim [[15]] 30, wherein the thickness of the silicon layer is about 50 to 500 .ANG..

23. (currently amended)The method as claimed in claim [[15]] 30, wherein the copper or copper alloy is formed by the steps of: depositing a copper seed layer in the opening; and electro-chemical plating or electroless plating the copper or copper alloy on the copper seed layer.

24. (currently amended)The method as claimed in claim [[15]] 30, wherein the copper or copper alloy is formed by chemical vapor deposition.

25. (currently amended)The method as claimed in claim [[15]] 30, wherein the copper silicide layer is formed by subjecting the semiconductor substrate to an inert gas-containing ambience at a temperature of about 150 degrees C. to about 450 degrees C.

26. (cancelled)

27. (currently amended)The method as claimed in claim [[15]] 30, wherein the diffusion barrier layer comprises silicon-rich oxide, SiN, SiC, SiOC, SiOCN, carbon-containing silicon oxide, or nitrogen-containing silicon oxide.

28. (currently amended)The method as claimed in claim [[26]] 30, further comprising a step of: forming an etch-stop layer overlaying the diffusion barrier layer.

29. (original) The method as claimed in claim 28, wherein the etch-stop layer comprises silicon-rich oxide, SiC, SiOC, SiON, SiOCN, carbon-containing silicon oxide or nitrogen-containing silicon oxide.

30. (currently amended) A method for fabricating a semiconductor device, comprising:
forming a dielectric layer overlaying a semiconductor substrate;
forming an opening in the dielectric layer;
embedding copper or copper alloy into the opening;
forming a silicon layer on the copper or copper alloy; [[and]]

reacting the silicon layer with the underlying copper or copper alloy to form a copper silicide layer capping the surface of the copper or copper alloy;

removing un-reacted portions of the silicon layer; and

forming a diffusion barrier layer overlaying the copper silicide.